

IN THE UNITED STATES

PATENT AND TRADEMARK OFFICE

APPLICANTS: James D. Kelly *et al.*
APPLICATION NO.: REISSUE OF USPN 5,996,036
FILING DATE: HERewith
TITLE: BUS TRANSACTION REORDERING IN A COMPUTER SYSTEM HAVING
UNORDERED SLAVES
EXAMINER: UNASSIGNED
GROUP ART UNIT: UNASSIGNED
ATTY. DKT. NO.: 18602-06222

BOX REISSUE
U.S. PATENT & TRADEMARK OFFICE
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**PRELIMINARY AMENDMENT AND
STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES
UNDER 37 CFR § 1.173(c)**

Sir:

Prior to examination of the subject reissue patent application, please amend the patent as indicated below:

IN THE SPECIFICATION

Insert at column 1, line 4, the following sentence:

This application is a continuation-in-part of U.S. Patent Application No. 08/432,622, filed May 2, 1995, now abandoned.

IN THE CLAIMS

Add claims 18-19, as indicated below:

18. A method of avoiding deadlock in a computer system having a split-transaction bus and a single-envelope bus bridged by a bus bridge, the split-transaction bus and the single-envelope bus each having at least one master device and one slave device connected thereto, comprising:

storing data from one or more accepted bus transactions;
determining, prior to a request for a bus transaction from a requestor, if execution of such
bus transaction would cause deadlock based on the stored data; and
responsive to the determination that execution of the bus transaction would cause
deadlock, sending a retry signal to the bus transaction requestor.

19. An apparatus for avoiding deadlock in a computer system having a split-transaction bus and a single-envelope bus bridged by a bus bridge, the split-transaction bus and the single-envelope bus each having at least one master device and one slave device connected thereto, comprising:

a memory for storing data from one or more accepted bus transactions; and
deadlock avoidance logic coupled to the memory for determining, prior to a request for a
bus transaction from a requester, if execution of the bus transaction would cause
deadlock based on the stored data, the deadlock avoidance logic adapted to send a
retry signal to the bus transaction requester if execution of the bus transaction would
cause deadlock.

STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES

Original claims 1-17 are in the patent as issued and new claims 18-19 are pending. Support for new claims 18-19 can be found in the specification of the issued patent at cols. 9-11 *et seq.* and cols.18-19 *et seq.*

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